REMARKS

STATUS OF THE CLAIMS

Claim 6 is added.

Claims 1-5 are rejected.

Claims 1-6 are currently pending.

ITEM 1: OBJECTIONS

In the foregoing, the claims are amended responsive to the objectives and helpful suggestions of the Examiner to overcome the objections, and it is respectfully submitted the objections are overcome, and accordingly, should be withdrawn.

ITEM 2: REJECTION OF CLAIMS 1 AND 5 UNDER 35 U.S.C. 112, SECOND PARAGRAPH, FOR INDEFINITENESS

The rejection is respectfully traversed.

The Examiner cites solely the opening phrase of the preamble of claims 1 and 5 in asserting the claims do not define "when or how the clock signals are synchronized," and the Examiner completely ignores the recitations of the respective bodies of claims 1 and 5, which define how the clock signals are synchronized.

The Examiner is respectfully reminded that the test for definiteness is whether one skilled in the art would understand the bounds of the claim when read in light of the specification. See MPEP 1504.04. Accordingly, if the claims read in light of the specification reasonably apprise those skilled in the art of the scope of the invention, 35 USC 112 demands no more.

The Applicants respectfully submit that the specification sets forth examples of a DPLL (Digital Phase Locked Loop) known in the art, which defines how clock signals are synchronized. The specification at page 2, lines 28-32 describes in one instance a conventional phase comparing part comparing a read clock signal RCLK with a write clock signal WCLK, and delivering a phase comparison signal to the DPLL to synchronize the read clock signal RCLK with the write clock signal WCLK. Another instance known in the art, which defines how clock signals are synchronized, is described in the specification on page 3, lines 10-26.

Furthermore, FIGS. 2 and 3 of the present application illustrate an embodiment of present application describing a DPLL circuit and a phase comparison result detecting part,

respectively. FIG. 2 clearly shows a phase comparing part 1 receiving signals ACLK and BCLK (input and output clock signals respectively) as input, and outputting a phase comparison signal PC. FIG. 3 clearly shows a synchronizing part 11 of the phase comparison result detecting part synchronizing the phase comparison signal PC with a master clock signal, and thereafter generating a synchronization signal.

Accordingly, the Applicants respectfully submit that the recitations within claims 1 and 5, when read in light of the specification, and as understood by a person of ordinary skill in the art, define how and when the clock signals are synchronized.

In view of the above, it is respectfully submitted that the rejection of claims 1-5 is overcome, and accordingly, should be withdrawn.

ITEM 3: REJECTION OF CLAIM 5 UNDER 35 U.S.C. 103(A) AS BEING UNPATENTABLE OVER LEE (USP 5,781,054) IN VIEW OF GARLEPP ET AL. (USP 6,920,622)

The rejection is respectfully traversed.

The amendment to claim 5 is supported by FIG. 7 and the associated description. Particularly, the illustration of FIG. 7 provides support for a plurality of mask rates.

Garlepp does not disclose, "a mask processing part identifying a single applied mask rate among a plurality of mask rates for masking a part of an increasing/decreasing (INC/DEC) request signal depending on a phase difference between the input clock signal and the master clock signal, masking the output signal from the phase comparison result detecting part depending on the identified mask rate, and outputting the masked signal," as recited in currently amended claim 5. Although Garlepp discloses a spilt/swallow control signal, Garlepp does not describe, "identifying a single applied mask rate among a plurality of mask rates for masking a part of an increasing/decreasing (INC/DEC) request signal" as recited in currently amended claim 5.

Accordingly, currently amended claim 5 distinguishes over the combination of Lee and Garlepp, et al.

In view of the above, it is respectfully submitted that the rejection of claim 5 is overcome, and accordingly, should be withdrawn.

NEW CLAIM 6

It is respectfully submitted that new claim 6 distinguishes over the art and rejection of record. Particularly, none of the cited references disclose or suggest an "execution rate computing part," and a "clock generating part including a INC/DEC request mask control means" as recited in claim 6.

CONCLUSION

In view of the above, it is respectfully submitted that the application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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